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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,165	09/18/2003	J. Young J. Paik	007734 FPS/MMCS/APC/DV	6290

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EXAMINER
MACARTHUR, SYLVIA

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/665,165	PAIK, J. YOUNG J.
	Examiner	Art Unit
	Sylvia R. MacArthur	1763

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _18 September 2003_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _18 September 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   Claims 1,2,4, 6,10, 12, 13, 15,17, 19, 23-26, 29, and 30 are rejected under 35 U.S.C.

103(a) as being unpatentable over Bennett et al (US 7,024,268) in view of Lee et al (US

6,517,412).

Bennett teaches a feedback controlled polishing process wherein a wafer comprising a plurality

of layers is polished, see col. 4 lines 43-51.

Regarding claim 1:Bennett et al teaches a computer-implemented method for updating a process

recipe in a CMP process for a wafer comprising the steps of:

(a) inputting a model for CMP processing of a wafer with a plurality of layers said model

comprising a first component that predicts a value for a characteristic (film thickness)

(b) determining a process recipe based upon the model of step (a);

(c) receiving a measured value of the characteristic thickness according to the process recipe of

step(b); and

(d) determining an updated model based upon the difference between the measured value

and the predicted value of the characteristic.

Bennett et al fails to teach determining a process recipe and using the results for a subsequent wafer.

Lee et al teaches using a CMP process recipe for a subsequent wafer.

The motivation to modify the controller of Bennett et al to use the step of using the data for a susbsequent wafer is that it provides the means to measure and control the thickness of a plurality of layers of a wafer within an entire lot without having to reprogram wafer to wafer.. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to use the algorithm of Bennett et al with the teachings of Lee et al to increase throughput.

Regarding claim 2: The method of claim 1, wherein the model of Bennett et al determines a first process recipe for the first layer of the wafer and a second process recipe for the second layer of the wafer, see cols. 7 and 8.

Regarding claims 4 and 15: The method of claim 1, wherein the characteristic of the first and second layers of the wafer comprises film thickness, and/or the control parameter comprises polishing time, the characteristic discuss in Bennett et al see col. 4 lines 44-52.

Regarding claim 6: The method of claim 1, wherein the processing recipe comprises a plurality of polishing steps, see Campbell et al col. 6 lines 34-37.

Regarding claims 10 and 23: A method (or apparatus) of controlling a characteristic of a wafer in a CMP operation, comprising the

steps of:

(a) providing a model for CMP processing of a wafer having at least first and second layers comprising at least one control parameter capable of being controlled, comprising a

(b) polishing a wafer using a first polishing recipe based upon the model of step (a);

(c) measuring the wafer characteristic for a wafer processed according to the process

recipe of step (b); and

(d) determining an updated model based upon the difference between the measured value

and the predicted value of the wafer characteristic, see col. 6 lines 4-21 and 50-57.

Regarding claims 12 and 24. The method of claim 10, wherein the model determines a first

process recipe for the first layer of the wafer and a second process recipe for the second layer of

the wafer, see Fig. 1 of Bennett et al.

Regarding claims 17 and 28: The polishing process comprises a plurality of polishing steps see

Bennett et al Fig.1.

Regarding claims 19 ,26, and 29: The polishing of step (b) comprises polishing the wafer at a

plurality of polishing stations, see Fig. 2 of Bennett et al and the paragraph joining cols. 3 and 4.

Regarding claim 30: An system for polishing a wafer in a CMP operation having controlled

characteristics, comprising:

(a) a model for comprising at least one control parameter capable of being controlled for

CMP processing of a wafer having at least first and second layers, comprising a first

component that predicts a value for a characteristic of the first layer and a second component

that predicts a value for a characteristic of the second layer;

(b) CMP polishing station for polishing a wafer using a first polishing recipe based upon

the model of step (a);

(c) a metrology tool (see col. 4lines 7-26 and col. 8 lines 21-44) of Bennett et al for measuring

the wafer characteristic for a wafer processed according to the process recipe of step (b); and

(d) a computer 90 for calculating an updated model based upon the difference between the

measured value and the predicted value of the wafer characteristic.

Bennett e al teaches a method for determining a polishing recipe based upon the measured pre-

polished thickness of a process layer.

3.   Claims 3,5,7-9, 11, 14, 16, 18, 20-22, 27, and 28 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Bennett et al in view of Lee et al as applied to claims 1,2,4, 6,10, 12, 13,

15,17, 19, 23-26, 29, and 30 above, and further in view of Campbell et al (US 6,230,069 also

known as Campbell et al '069).

The teachings of Bennett as modified by Lee et al were discussed above.

Neither teaches a specific model for the wafer characteristics.

Campbell et al teaches system and method for controlling a CMP polishing tool, see abstract.

Regarding claims 3 and 14. The model is defined as:

$Yt = YA + Ys,$

where

Yt is the model for a CMP process for a multi-layer wafer;

YA is the model for a CMP process for the first layer of the wafer; and

YB is the model for a CMP process for the second layer of the wafer.

This a short hand version of equation 13 of Campbell et al US 6,230,069)

The motivation to modify the method of Bennett in view of Lee which suggest a CMP process

recipe for processing wafer having a plurality of layers and using the data for subsequent wafers

with the specific model of Campbell is that it provides the optimal linear approximation of a

CMP process having the variables stated above. Therefore, it would have been obvious for one

of ordinary skill in the art at the time of the claimed invention to provide the model equation of

Campbell in the method of Bennett in view of Lee et al.

Regarding claims 5, 16,18, and 27: The method of claim 1, wherein the model of step (a) defines

a plurality of regions on a

wafer and a measured value for the wafer characteristic for each of the plurality of

regions is received in step , (c), the values a, b of equation 7 take into account the topography of

the wafer according to col. 5 lines 20-25 of Campbell et al '069.

Regarding claim 7: The method of claim 1, wherein the model accounts for a tool state of a tool

used in the CMP processing of a wafer, see col. 2 lines 55-67

Regarding claim 8:. The method of claim 1, further comprising developing a model, said model

development

comprising the steps of

 (e) inputting pre-polished wafer characteristics for one or more wafers;

(f) receiving measured values of the wafer characteristics for the one or more wafers

processed according to a processing recipe;

(g) providing a model defining the effect of tool state on polishing effectiveness; and

 (h) recording the pre-polished and post-polished wafer characteristic on a recordable

medium, see col.4 lines 22-46 of Campbell et al '069.

Regarding claim 9: The method of claim 8, wherein model development further comprises fitting

the data to a curve that establishes a relationship between the wafer characteristic and the control

parameter, see col.7 lines 10-19 of Campbell et al '069.

Regarding claims 11 and 20: The method of claim 10, further comprising:

determining an updated process recipe based upon the updated model of step (d) see col.6 lines

24-60 of Campbell et al '069.

Regarding claims 13, 21, and 25: The method of claim 10, wherein the model accounts for the

tool state of a tool used in the CMP processing of a wafer, see abstract of Campbell et al '069.

Regarding claim 22: The method of cla im 19, wherein, the initial wafer thickness for each of the

polishing stations is provided by the prediction from previous polishing stations, factor a

considers tool shift, see col. 5 lines 7-19 if Campbell et al '069.

Response to Arguments

4.   Applicant's arguments with respect to claims 1-30 have been considered but are moot in

view of the new ground(s) of rejection. The prior art of Bennett teaching a process recipe for

CMP on multilayered wafers which enhances its recipe with a teaching of increased throughput

by Lee et al.

Conclusion

5.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. The amendment requiring the recipe provide polishing of a plurality of wafers on

the same substrate necessitated the introduction of the prior of Bennett et al and Lee et

alAccordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is

reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Conclusion

6.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Sylvia R. MacArthur whose telephone number is 571-272-1438.

The examiner can normally be reached on M-F during the hours of 8:30 a.m. and 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sylvia R MacArthur
Patent Examiner
Art Unit 1763

June 12, 2006

PARVIZ HASSANZADEH
SUPERVISORY PATENT EXAMINER